



AI for Fully-Automated Chip Design: ***The Times They Are a-Changin'***

Institute of Computing Technology, Chinese Academy of Sciences

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2024: Gimmick or Trend

[AI for Automated Chip Design: Everything, Everywhere, All at Once \(?\)](#)

David Pan, The University of Texas at Austin

[Automatically generating robotics accelerators](#)

Yuhao Zhu, University of Rochester

Break

[A Systematic and rapid approach to design space exploration for tensor accelerators](#)

Qijing Huang, NVIDIA

[Empowering Physical Design of VLSI Circuits with Deep Learning: from Modeling to Optimization](#)

Yibo Lin, Peking University

[Machine Learning for System-Level Design: Challenges and Opportunities](#)

Andreas Gerstlauer, The University of Texas at Austin

[Chip Learning for Processor Design](#)

Zidong Du, Institute of Computing Technology, Chinese Academy of Sciences

[Scaling Up the Hardware Design Capability of LLMs: Lessons from the 1st OpenDACs Contest of Processor Design](#)

Cangyuan Li, Institute of Computing Technology, Chinese Academy of Sciences

[A High-Level Synthesis Based Framework for Design Space Exploration and Generation of Neural Network Accelerators](#)

Kartik Prabhu, Stanford University

[Machine Learning Assisted Memory and Storage System Management](#)

Onur Mutlu, ETH Zurich

2025: The Times They Are a-Changin'

[Hypothesizing \(Fantasizing\) Autonomous Hardware Design](#)

Zhiru Zhang, Cornell University

[The Role of AI for Next Generation SW/HW Codesign](#)

Vincent T. Lee, Meta

[QiMeng: Automated Hardware and Software Design for Processor Chip](#)

Di Huang, Institute of Computing Technology, Chinese Academy of Sciences

[Hair of the Dog: How AI Can Help Formally Verify AI-Designed Chips](#)

Yatin Manerkar, University of Michigan

[Learning with Limited Resources: Optimizing Neural Networks for Extreme Efficiency](#)

Radu Marculescu, University of Texas at Austin

Break

[hdl2v: A Code Translation Dataset for Enhanced LLM Verilog Generation](#)

[Towards an Agile and Autonomous Verification Framework for AI-Generated Chip Designs](#)

[Leveraging Large Language Models for Coverage-Driven Verification of Open-Source RISC-V Cores](#)

[ProtoCoLLM: RTL Benchmark for SystemVerilog Generation of Communication Protocols](#)

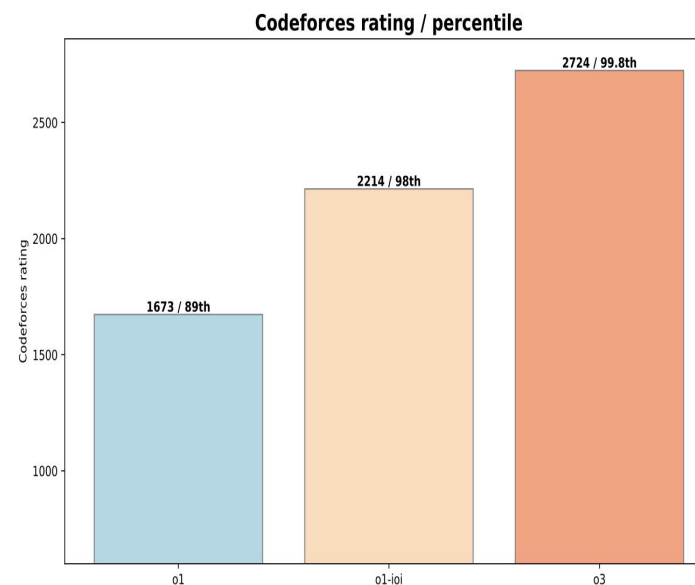
[ChiselLLM: Unleashing the Power of Reasoning LLMs for Chisel Agile Hardware Development](#)

The Breakout Year for Reasoning Models

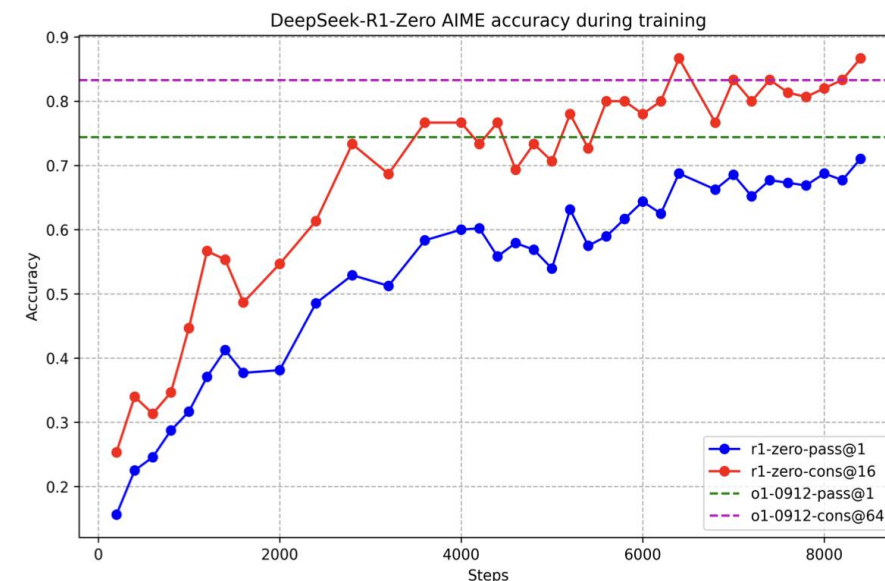
AlphaProof winning a silver medal at the IMO 2024



O3 achieved Gold; 99.8th in Codeforces



DeepSeek R1: Self-emergence of reasoning



Processor Design: Apex of Logic Reasoning



Alonzo Church
**one of the
founders of
the computer
science**

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[11] and available code for the number n . (Both f and n are variables here.) Then the machine is to go to work and is to produce a code for a number m and only if $f(m)$ is defined, and if $f(m)$ is defined the coded number is to be $f(m)$. (2) Similar to (1) but now the machine is to reproduce on the tape not only $f(m)$ but the coded formal all steps that the machine with the program [11] would go through in computing $f(m)$ from m .

The author asserts that problem (1) can be solved because, using the standard notation and terminology for recursive functions introduced by Kleene, / has a Gödel number x and $f(m)$ is defined $f(m) = (Ux)(Uy, m, y)$. So if one constructs the program for determining $(Ux)(Uy, m, y)$ one has solved (1). Problem (2) is said to be more difficult and the second paper is mostly devoted to constructing a detail n more difficult (2). It is assumed that the reader knows that there are no machines that machine II goes through when programmed by [11] and fed n on the tape is also a partial recursive function of [11] and n . (2) could be solved for a short argument like that used in (1).

STEVEN CHAY

Abstracts. *Application of recursive arithmetic to the problem of logical synthesis.* *Summaries of talks presented at the Summer Institute for Symbolic Logic, Cornell University, 1955, 2nd edn., Communications Research Division, Institute for Defense Analysis, Princeton, N. J., 1960, pp. 2-85, 26-45b.*

In this early paper on the application of formal logic to circuits and automata Church develops and extends a theory of restricted recursive arithmetic first presented in his review (RSK 288) of an article by B. C. Berkeley. The author here presents several alternatives for the recursive schemata of that system. Let $x = (x_1, \dots, x_k)$, $y = (y_1, \dots, y_l)$. The schemata for restricted recursion (A) are

$$r_0(x) = P_0(x_0)$$
$$r_i(x) = 1 + Q_i(x_0, x_1 + 1, r_0)$$
$$i = 1, \dots, k$$

and for wider restricted recursion (B) are

$$r_0(x) = P_0(x_0), \dots, r_k(x) = P_k(x_0, \dots, x_k)$$
$$r_i(x + k + 1) = Q_i(x_0, \dots, x_i + 1, r_0, \dots, r_{i-1}, r_i + k_1)$$

for sequential auxiliary recursion (C), the schemata are the same as for (B) except that $r_0(x) = P_0(x_0, \dots, x_k)$ for $j = 0, \dots, k$.

It is shown that recursive and finite schemata can be treated by means of restricted recursive arithmetic (A), or by (B), which is reducible to (A).

Two problems for recursive arithmetic are studied. The *constructive problem* gives a requirement $R(x)$ in a logical system which is an extension of recursive arithmetic, to find if possible recursive expressions for a circuit which satisfies the requirement. And the *decision problem* gives both requirement and recursion equivalence, to determine whether the circuit satisfies the requirement.

The systems problem is solved first for the case of one free variable (Case 1).

$$R(x_0), \dots, R(x_k), r_0(x), \dots, r_k(x) = Q_0(x_0, \dots, x_k), r_0(x), \dots, r_k(x) + k_1$$
$$f = 1, \dots, k, \quad f = 1, \dots, k$$

The synthesis method contains within it a test to determine if a solution is possible. An alternative treatment of this synthesis problem is included by Wang in RSK 273.

Case 2 of the systems problem, a requirement with two or more free variables is solved by reduction to Case 1. Case 3, a requirement with quantifiers, is treated by using Berkeley's procedure to limit the scope of each quantifier. Several subcases of Case 3 are solved, but the complete solution is not obtained. Case 4, in which the requirement includes $=$ and $<$, is proposed and a conjecture given about a possible method of solution. An additional case, in which the requirement contains $+$, $=$ and

[A. Church 1957]



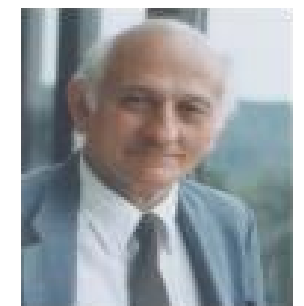
Church' s Problem: **Given**
input and output bitstreams α
and β , automatically construct
a circuit design that describes
the input-output relationship.



R. Floyd
Automatic program
synthesis and
verification



J. Hopcroft
Logic synthesis

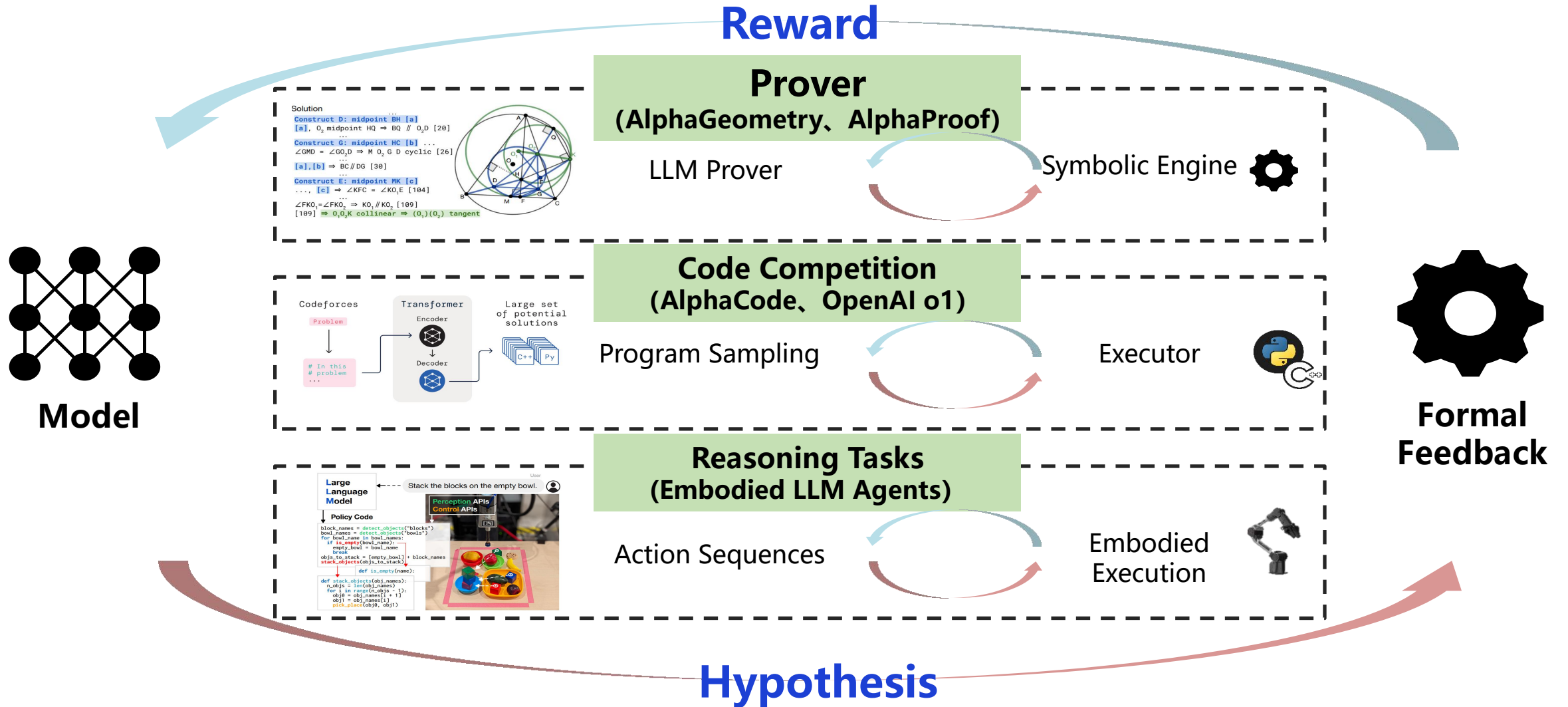


J. Cocke
Circuit design

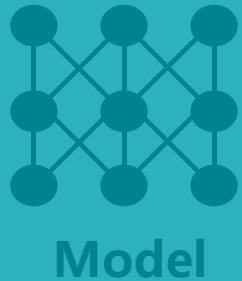


1957: The Church' s problem of automatic circuit design

Pradigm of Reasoning Tasks

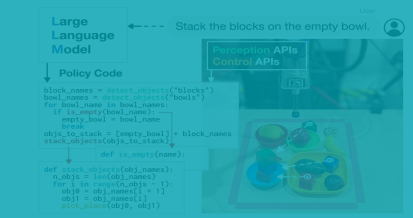
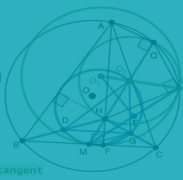


Pradigm of Reasoning Tasks



Design

Solution
Construct D: midpoint BH [a]
[a], O, midpoint HQ \Rightarrow BQ // O.D [26]
Construct G: midpoint HC [a] ...
 $\angle GMD = \angle GPD \Rightarrow$ M O, G D cyclic [26]
[a], [b] \Rightarrow BC // DG [30]
Construct E: midpoint MK [a]
... [a] \Rightarrow $\angle KFC = \angle KOE$ [104]
 $\angle FKO = \angle FKO \Rightarrow$ KO // KO, [109]
[109] \Rightarrow O, O, K collinear \Rightarrow O, (O, K) tangent



Reward

Prover

(AlphaGeometry, AlphaProof)

LLM Prover

Code Competition
(AlphaCode, OpenAI o1)

Program Sampling

Reasoning Tasks
(Embodied LLM Agents)

Action Sequences

Hypothesis

Symbolic Engine

Verification

Formal Feedback

Embodied Execution

Talk Overview

SW/HW Co-design

The Role of AI for Next Generation SW/HW Codesign

Design

ProtocolLLM: RTL Benchmark for SystemVerilog Generation of Communication Protocols

ChiseLLM: Unleashing the Power of Reasoning LLMs for Chisel Agile Hardware Development

Boosting

hdl2v: A Code Translation Dataset for Enhanced LLM Verilog Generation

Feedback-driven Loop

Hypothesizing (Fantasizing)
Autonomous Hardware Design

QiMeng: Automated Hardware
and Software Design for Processor
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Verification

Hair of the Dog: How AI Can Help Formally Verify AI-Designed Chips

Leveraging Large Language Models for Coverage-Driven Verification of Open-Source RISC-V Cores

Boosting

Data, Infrastructure, Tools

Learning with Limited Resources: Optimizing Neural Networks for Extreme Efficiency

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